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Design of All- Digital Phase-Locked Loop Applied To Grid Connected Power Converter

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Abstract— ***Applications of grid connected power converter are growing rapidly. Unique properties of Synthetic All-digital phase locked loop(ADPLL) system are widely used in various applications* like frequency synthesizer, *frequency modulators & demodulators or phase modulators & demodulators in data communication systems, clock recovery circuits in disk drives and velocity detectors in motor drive systems. ADPLL is one of the most flexible and reliable system for grid connected power converter applications. The frequency and phase angle of the utility voltage are crucial for the proper operation of most grid-connected power converters in distributed generation systems (DGS), flexible ac transmission systems and uninterruptible power supplies and is usually needed for the synchronization of the converter output voltages, for power flow calculations or for the transformation of state variables into rotating reference frames. The objective of this paper includes the designing of ADPLL system and the designed ADPLL is proposed for grid interface power converters to detect the frequency & phase angle and for generating a synchronized output signal which is in synch with input signal with respect to frequency as well as in phase. The proposed ADPLL reduces the output jittering, cost, Phase error, computational hardware requirements, complexity of a system and increases the track in range, lock in range, speed of the system. This designed ADPLL is proposed for grid interface converters to detect the frequency & phase angle .The main design of this paper is implemented in XILINX. Developed using VERILOG language. Also a few block enhancement features facilitates in the designing and producing desired output.***

Keywords-— All-Digital Phase-Locked Loop (ADPLL), Grid connected power converters, positive- and negative-sequence separation, Distributed generation system (DGS).

Introduction

The Phase Locked Loop (PLL) is an extremely versatile circuit used in electronic communication systems like modulator, demodulator, carrier & clock recovery, frequency generator and frequency synthesizer. Frequency synthesizer is used to generate many output frequencies through addition, subtraction, multiplication, division of small number of fixed frequency sources. It is a crystal controlled variable frequency generator. Various applications of frequency synthesizers are in test and measurement equipments (Audio and RF signal generator), touch tone, remote control unit (electronic tuners), multichannel communication systems (telephony) and music synthesizers. The frequency and phase angle of the utility voltage are crucial for the proper operation of most grid-connected power converters in distributed generation systems (DGS) [1], Flexible AC transmission systems [2] and Uninterruptible power supplies [3]. The information is usually needed for the synchronization of the converter's output voltages, for power flow calculations and for the transformation of state variables into rotating reference frames [4]–[6].

The frequency and angle information are typically extracted using phase-locked loops (PLLs). A popular way to implement the PLL is to construct it with digital and the phase angle can be detected based on the zero crossings of the input voltage or current [7]. This type of PLL is attractive to the industry because of the lower cost, better stability and less computational requirement [8]. However, it also has disadvantages such as slow tracking speed, narrow lock-in range, high pulse jittering, and sensitivity to grid disturbance [9]. Another type of PLL is implemented in software [in a digital signal processor (DSP)] using utility voltage information. In three-phase systems, the software-based PLLs are usually implemented in the synchronous reference frame (SRF) [10], [11]. By reducing the bandwidth, the SRF PLL can also operate in grid unbalanced conditions. But this is an inefficient solution [12]. The performance of SRF PLL under distorted or unbalanced utility voltages can be improved by applying digital filters and separating the positive and negative sequence components [1], [13], [14]. In order to improve the dynamic performance of the PLL during voltage unbalance, a software-implemented second-order generalized integrator (SOGI) PLL is proposed in [4]. Compared with the traditional DPLL, software-based PLL is more flexible and effective. Particularly under circumstances such as the fault

ride through control of the DGS where grid disturbance exists.

I. PROPOSED SYSTEM

All –digital Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. In this design ADPLL implemented as digital circuit. Both analog and digital PLL circuits include same basic elements:

Phase detector

Input fault detector

Up/down counter

RACC

Period detector

Variable detector

Input fault detector

External counter

Digital VCO

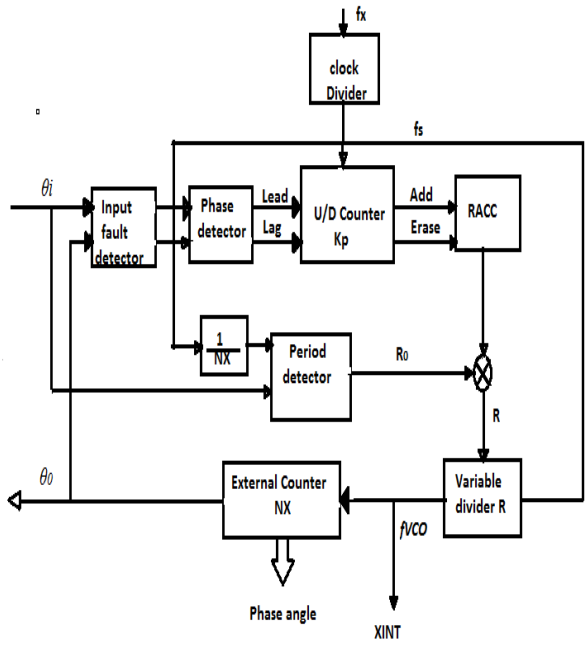

Fig.1, Block diagram of proposed ADPLL

The block diagram of the proposed ADPLL is shown in Fig. 1.The input fault detector has two states 0 and 1. Where 0 states incoming signals as analog & state 1 indicates the signal as digital.

PD is a XOR gate which compares the phases of the input and output signals in each period. It outputs the lead signal if the phase of the input signal precedes the output signal or outputs the lag signal if this phase lags behind.

The U/D counter, with a modulus *Kp* functions as a digital filter and is controlled by the output signal of the PD. When the output of the PD is a lag signal, the U/D counter counts up by the number of pulses of the system clock corresponding to the phase difference. Conversely, it counts down when the output signal is lead. A carry signal (erase signal) is produced if the counter value of the U/D counter exceeds *Kp* and a borrow signal (add signal) is generated when the U/D counter counts down to zero.

The circuit removes one pulse from the output clock whenever the signal from the U/D counter is erase signal and adds one pulse for the add signal. The output clock with the erased or added pulses are further divided by *R* and then fed back to the PD.

The U/D counter controls a resettable accumulator (RACC), thus changing the divider ratio. The RACC counts the carry or borrow signal from the U/D counter and its output is limited to avoid any overflow in the following digital adder. By using a feed forward loop, the period of the input signal is detected and converted to be the center divider ratio *R*0, which is subsequently added to RACC.

The output of the adder is then used to control the digital voltage-controlled oscillator (VCO) frequency by varying the divider ratio *R*. The VCO output is divided by an external *Nx* counter and then fed back to the PD. The phase information of θi can be calculated from the value stored in the *Nx* counter.

The input frequency can also be calculated by averaging the variable divider *R*. By properly choosing *Nx*, *f*VCO can be programmed to trigger the external interrupt of a microcontroller unit (MCU) at the desired phase angles. This feature implies that the ADPLL can be easily utilized to produce the synchronous PWMs for the high-power converters [15].

An example for the operation of the ADPLL with $Nx = 1$ is shown in Fig. 2. In each cycle, the divider *R* varies with the feed forward *R*0 and the output of RACC. The counting rate of the divider is a constant since the divider *R* is variable, which results in the uniform pulses of *f*VCO. Compared with the traditional DPLL, the proposed ADPLL is very suitable for grid-side converter control.

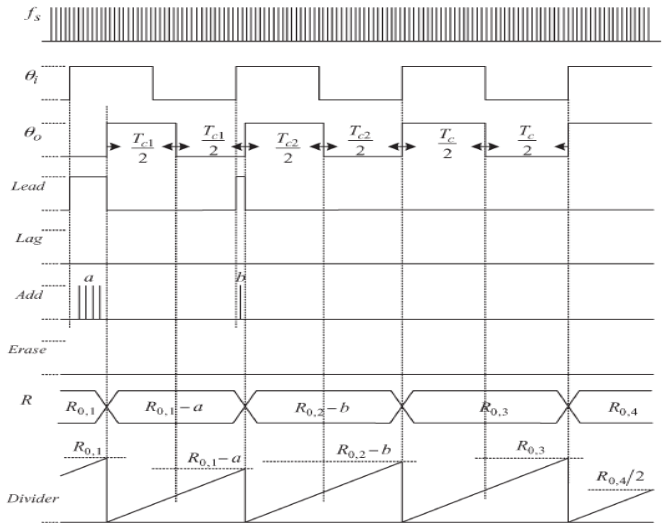

Fig 2 : Basic operation of proposed ADPLL

Where,
θi- Input phase angle
R0- Centre divider ratio
R –Variable divider ratio
Nx – Number of counts
fVCO - Frequency of VCO
a- Four clock pulse
b- One clock pulse

A. Comparison with traditional DPLL

The DPLL has a fixed divider ratio which makes the tracking range very narrow if a reasonable phase error is required for control purposes. The phase error of the traditional DPLL changes in accordance with the difference between the input frequency and the PLL center frequency. The phase error is not predictable if the input frequency is unknown. The phase information can't be obtained from the *Nx* counter. Because the pulse fed to the counter is not uniform. Most of all, the tracking speed is not acceptable, which is inversely proportional to the tracking range and phase error. In the proposed ADPLL with the input frequency feed forward loop, center frequency is always tracking the input frequency. The steady-state phase error and pulse jittering are therefore greatly reduced within two cycles of the fixed clock. Both are very small when the clock frequency is very high [9], [18]. Due to the variable divider ratio, the proposed ADPLL also features wide track-in range and fast pull-in time as concluded in [9]. With the feed forward loop, the pull-in time of the proposed ADPLL is even faster.

III. IMPLEMENTATION IN APPLICATIONS WITH GRID DISTURBANCE

Some applications require the grid-connected power converters to maintain proper operation even under grid disturbance. Taking DGS as an example, transmission operators issue stringent grid codes regarding the interconnection of the DGS to the utility grid to obtain maximal benefits from the distributed resources. One important code is that DGS should be able to ride through grid disturbances and to provide necessary services in order to behave as a conventional power plant and hence, it can be used to support the utility in case of a fault. Different control strategies for DGS running under faulty grid conditions have been studied. Regardless of the technique used in the system control, PLL is always necessary for the grid synchronization.

For some advanced control schemes, PLL should have the ability to separate the positive and negative sequences of the grid voltage rapidly and accurately. The filter-based SRF PLL responds slowly for the sequence separation. A software-based SOGI PLL containing no filter is proposed for the sequence detection.

The SOGI PLL is based on the instantaneous symmetrical component method, in which the grid voltages in a stationary ($\alpha - \beta$) reference frame are delayed by 90◦ and employed in the sequence calculation. Similar to the so-called delayed signal cancellation method, the SOGI PLL responds much faster than the conventional PLL and therefore is suitable for applications with grid disturbance. In this section, the performance of the proposed ADPLL during grid disturbance is experimentally compared with that of the SOGI PLL.

In order to extract the positive and negative sequences, the instantaneous grid voltage should be detected. Based on the symmetrical components method, the positive- and negative sequence vectors can be expressed with the phase voltage vectors the positive and negative components of the grid voltage can be deduced from (1)

$$\begin{bmatrix} \vec{u}_+ \\ \vec{u}_- \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix}\begin{bmatrix} \vec{u}_a \\ \vec{u}_b \\ \vec{u}_c \end{bmatrix} \qquad (1)$$

The positive and negative voltage vectors, are expressed as

$$\overline{u^+} = \overline{u\alpha^+} + j u\beta^+ \quad \textbf{and} \quad \overline{u_-} = u\alpha_- + j u\beta_-$$

Where ,
a = e−j(2/3)π.
ua, ub, and uc = Instantaneous grid phase voltages
θa, θb, and θc = Phase angle of each phase voltage

$$u_{\alpha+} = \frac{1}{3}\left[u_a - \frac{1}{2}(u_b + u_c) + \frac{\sqrt{3}}{2}\left(\frac{u_b}{\sin\theta_b} - \frac{u_c}{\sin\theta_c}\right)\right] \qquad (2)$$

$$u_{\beta+}=\frac{1}{3}\left[-\frac{u_a}{\tan\theta_a}+\frac{1}{2}\left(\frac{u_b}{\tan\theta_b}+\frac{u_c}{\tan\theta_c}\right)+\frac{\sqrt{3}}{2}(u_b-u_c)\right] \quad (3)$$

$$u_{\alpha-}=\frac{1}{3}\left[u_a-\frac{1}{2}(u_b+u_c)-\frac{\sqrt{3}}{2}\left(\frac{u_b}{\tan\theta_b}-\frac{u_c}{\tan\theta_c}\right)\right] \quad (4)$$

$$u_{\beta-}=\frac{1}{3}\left[\frac{u_a}{\tan\theta_a}-\frac{1}{2}\left(\frac{u_b}{\tan\theta_b}+\frac{u_c}{\tan\theta_c}\right)+\frac{\sqrt{3}}{2}(u_b-u_c)\right] \quad (5)$$

For the real implementation, the trigonometric values in (2),(3),(4)and (5) can be obtained with a lookup table and a hysteresis limiter is employed to avoid division by zero problems.

θa, θb, and θc are detected by the ADPLL and then the positive and negative sequences can be obtained with a simple calculation in a low cost MCU.

The performances of the ADPLL and the SOGI PLL are studied with different types of grid faults.

1) Single-phase fault: Usually phase shift between the phases appears in such unbalanced fault. In this case, *ua* registers the drop amplitude from 100% to 15% with 30◦ lagging, while the other two phase voltages remain normal.

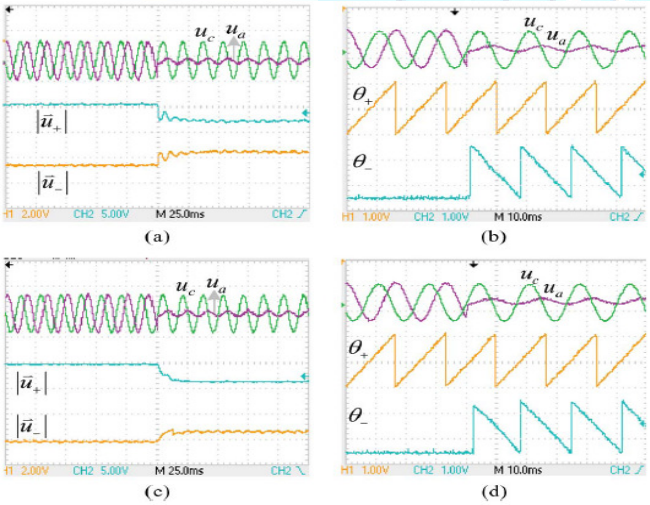

Fig 3: Positive and negative sequence detection during a single –phase fault
a) Voltage detected with ADPLL b) Phase angle detected with ADPLL c) Voltage detected with SOGI PL d) Phase angle detected with SOGI PLL

2) Two-phase fault: *ua* and *ub* register the drop amplitude from 100% to 15% with both 30◦ lagging, and *uc* remains normal.

3) Three-phase fault: All three grid voltages register the same drop amplitude from 100% to 15% with 30◦ lagging. The occurrence of this type of fault is extremely rare in power systems.

The experimental results: It shows that both ADPLL and SOGI PLL can be used in grid fault situations. With additional grid voltage information, the ADPLL functions as a software-based PLL, with which the positive and negative sequences can be separated. During the single-phase fault, the SOGI PLL responds smoother than the ADPLL because the phase shift in *ua* cannot be accurately identified by the ADPLL until the next zero-crossing point and the phase error results in the fluctuations of the positive and negative sequences.

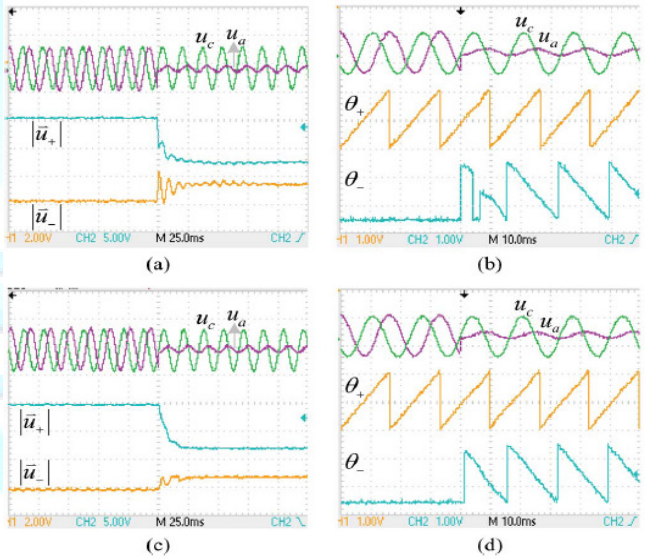

Fig 4: Positive and negative sequence detection during a two–phase fault a) Voltage detected with ADPLL b) Phase angle detected with ADPLL c) Voltage detected with SOGI PLL d) Phase angle detected with SOGI PLL

The situation is worse when a two-phase fault occurs with the phase shift as shown in Fig 5 . However, the value and phase angle of the voltage sequences are identified in two grid voltage cycles similar to the SOGI PLL. For the three-phase fault, the magnitude of the positive voltage $|\overrightarrow{u}_+|$ decreases dramatically, the negative voltage $|\overrightarrow{u}_-|$ is around "0 V" as the fault is symmetrical. It is noticed that the magnitude of $|\overrightarrow{u}_-|$ during the fault is different from the value under the normal grid voltage. The error comes from the asymmetry of the voltage sensor and the preprocessing circuits, which implies that the performances of both the ADPLL and the SOGI PLL are determined by the sensor resolution in the grid disturbance applications. However SOGI PLL depends more on the sensors and ADCs, for the phase angles of the voltage sequences are calculated based on the filtered instantaneous grid voltage and the input filter,

no matter if *RC* or digital filter, always provides delays on the voltage detection.

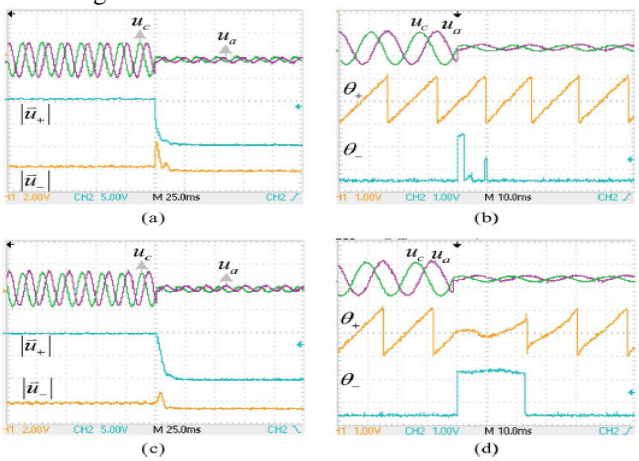

Fig 5: positive and negative sequence detection during a three–phase fault a) Voltage detected with ADPLL b) Phase angle detected with ADPLL.c) Voltage detected with SOGI PLL d) Phase angle detected with SOGI PLL

In contrast, the phase angles in the ADPLL are directly derived from the zero-crossing signal, which are not affected by the input filter. This small difference results in that the ADPLL has smaller dependence on the sensors. Although large overshoots appear in the detection results of the ADPLL due to the phase shift, the voltage sequences can be obtained after two input cycles as a similar performance to the SOGI PLL. It is expected that the sequence separation with the ADPLL may fail if a large amount of low-order harmonics exist in the grid voltages which distort the zero crossings. However, the SOGI PLL cannot work well in such situations either. In order to extend the PLL into such seriously distorted power system situations, assistant filters (software filters for the SOGI PLL and hardware filters for the ADPLL) are necessary.

IV RESULTS AND DICUSSIONS

Design of all digital phase locked loop to detect the frequency and phase angle of grid connected system. Also generating an output signal which is in synch with the input signal with respect to frequency as well as phase. The main design is implemented in XILINX 14.1i & is developed using VERILOG language. A few block enhancement features, which facilitates designing and producing desired output.

Simulation Results Using Xilinx

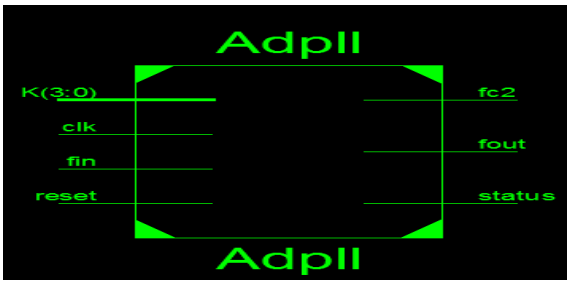

Fig 6:Main block of RTL schematic structure

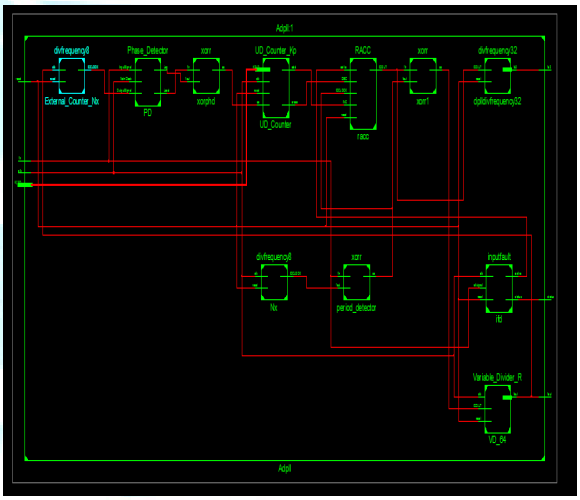

Fig 7: The RTL schematic view of ADPLL

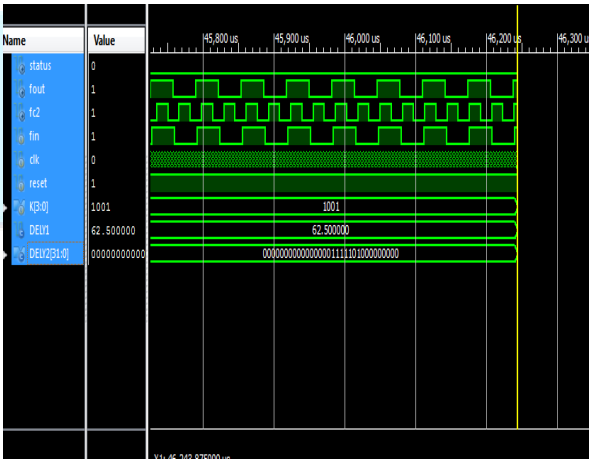

Fig 8: The simulated output

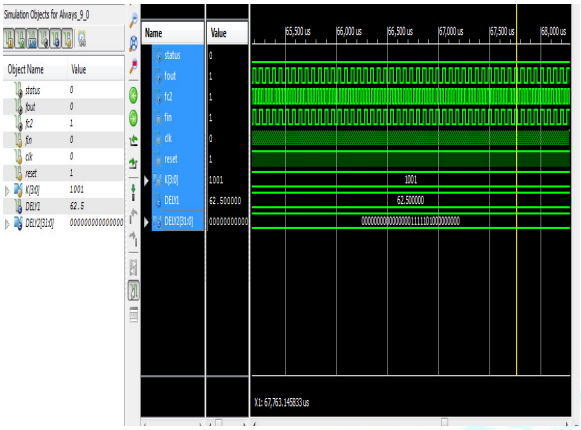

Fig 9: The main view of Simulated result

The DPLL, proposed ADPLL and SOGI PLL are compared in Table:1. It is noticed that the DPLL is the cheapest solution but the phase tracking performance is limited. In contrast, the ADPLL has a wider track-in time, faster pull-in time, negligible phase error and smaller output jittering. The performance of the SOGI PLL highly depends on the DSP performance and the accuracy of voltage sensors or ADCs since the phase value is derived from the software calculations based on the grid voltages. As a result, the cost of the SOGI PLL is the highest among the three PLLs.

Performance	DPLL	ADPLL	SOGIPLL
Hardware /software	Hardware	Hardware	Software
Cost	Very Low	Low	High
Track-In Range	Narrow	Wide	Depends On Sampling
Pull-In Time	>10 Periods	1 Period	1 Period
Phase Error	Large	Negligible	Depends On Sensor,ADC
Output Jittering	Large	Small	Depends On Sensor,ADC
Hardware Requirements	No	Voltage Sensors, ADC,MCU	Voltage Sensors, ADC,DSP
Calculation	NO	Simple	Complex

Sensitivity	Voltage Distortions	Voltage Distortions: Voltage Sensor and ADC	Voltage Distortions: Voltage Sensor and ADC
Application	1 Phase System: Symmetrical 3 phase system	1 Phase System: Symmetrical 3 phase system. Unsymmetrical 3 phase system Synchronous PWM	Symmetrical 3 phase system. Unsymmetrical 3 phase system

Table 1: Comparison with different PLL

Area Analysis using Xilinx

The schematic of area utilization design summary shown in the below Table:2 represents the how much of area used regarding of area allotted. In this project the number of Slice Flip Flops available is 3840 and used is 44 only. Therefore 1% of area is utilized. Similarly the other parameters related to area as shown below.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	44	3,840	1%	
Number of 4 input LUTs	132	3,840	3%	
Number of occupied Slices	78	1,920	4%	
Number of Slices containing only related logic	78	78	100%	
Number of Slices containing unrelated logic	0	78	0%	
Total Number of 4 input LUTs	132	3,840	3%	
Number of bonded IOBs	10	63	15%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	3.39			

Table 2: Device utilization summary

V.CONCLUSION

This paper concludes that the design of ADPLL has been proposed for grid-connected power converters. The frequency and phase angle of the grid voltage, which are usually detected by a PLL are important for the grid connection. The software-based PLL relies on the voltage detection and complex calculations. DPLL has a limited track-in range and large pulse jitter and is sensitive to grid disturbances. The proposed ADPLL has improved track-in range and lower output jitter due to a feed forward input

loop and a variable divider ratio. If additional voltage measurements are provided, the ADPLL can be applied to detect the positive and negative sequence voltages in the grid fault situation, which is experimentally verified to have similar performance to the SOGI PLL.The proposed ADPLL can also be directly utilized to generate the synchronous PWM for high power converters.

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